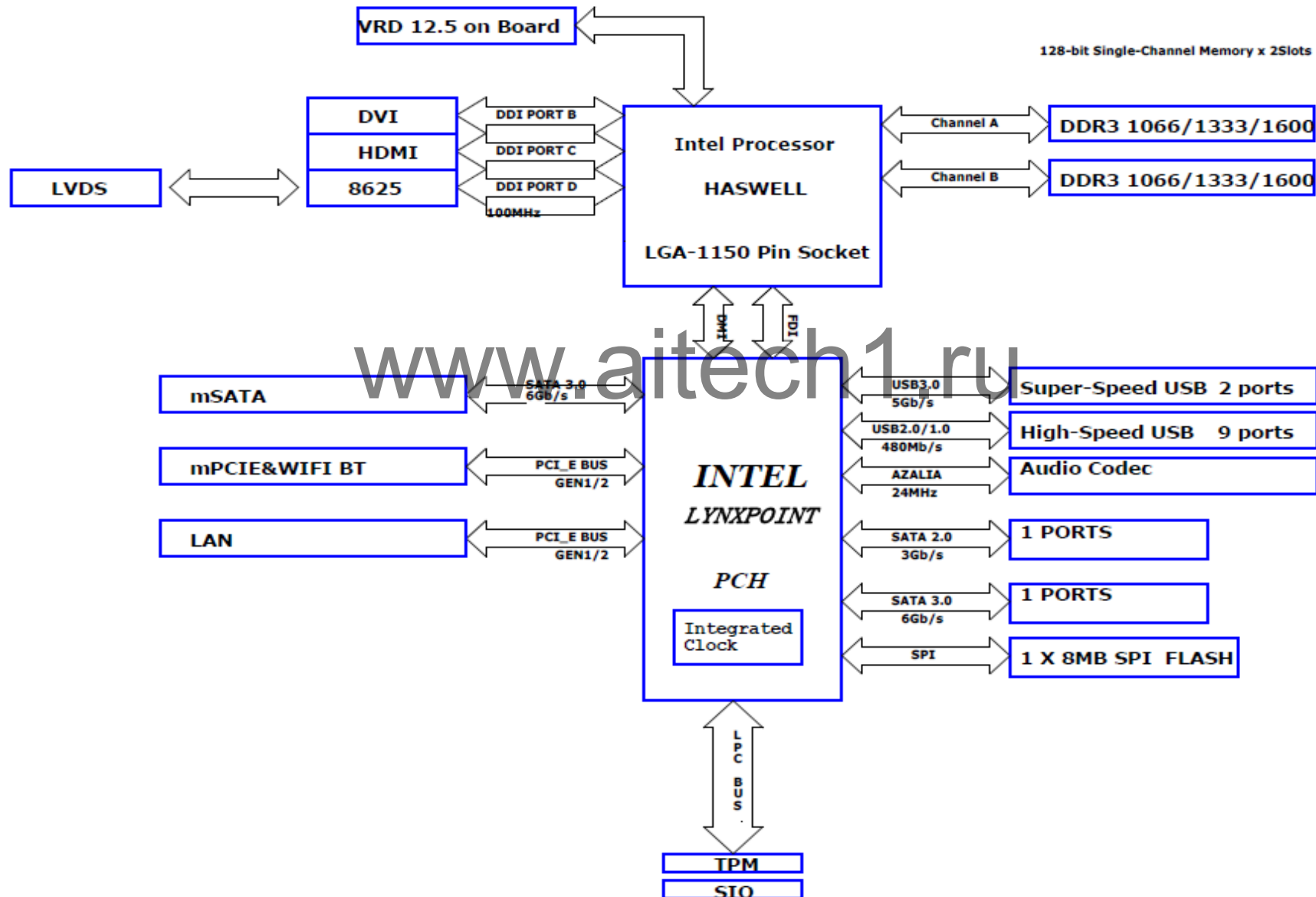
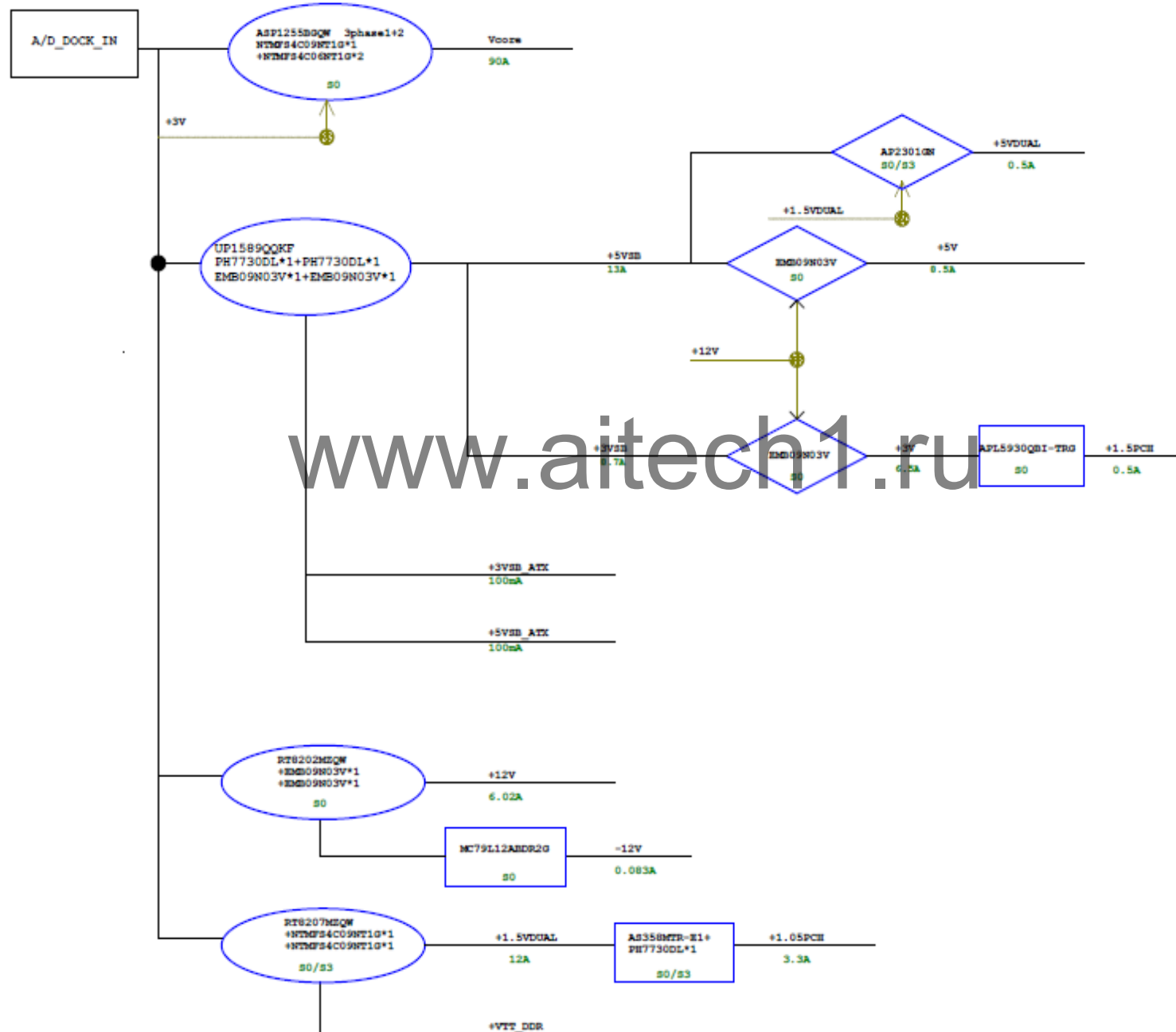


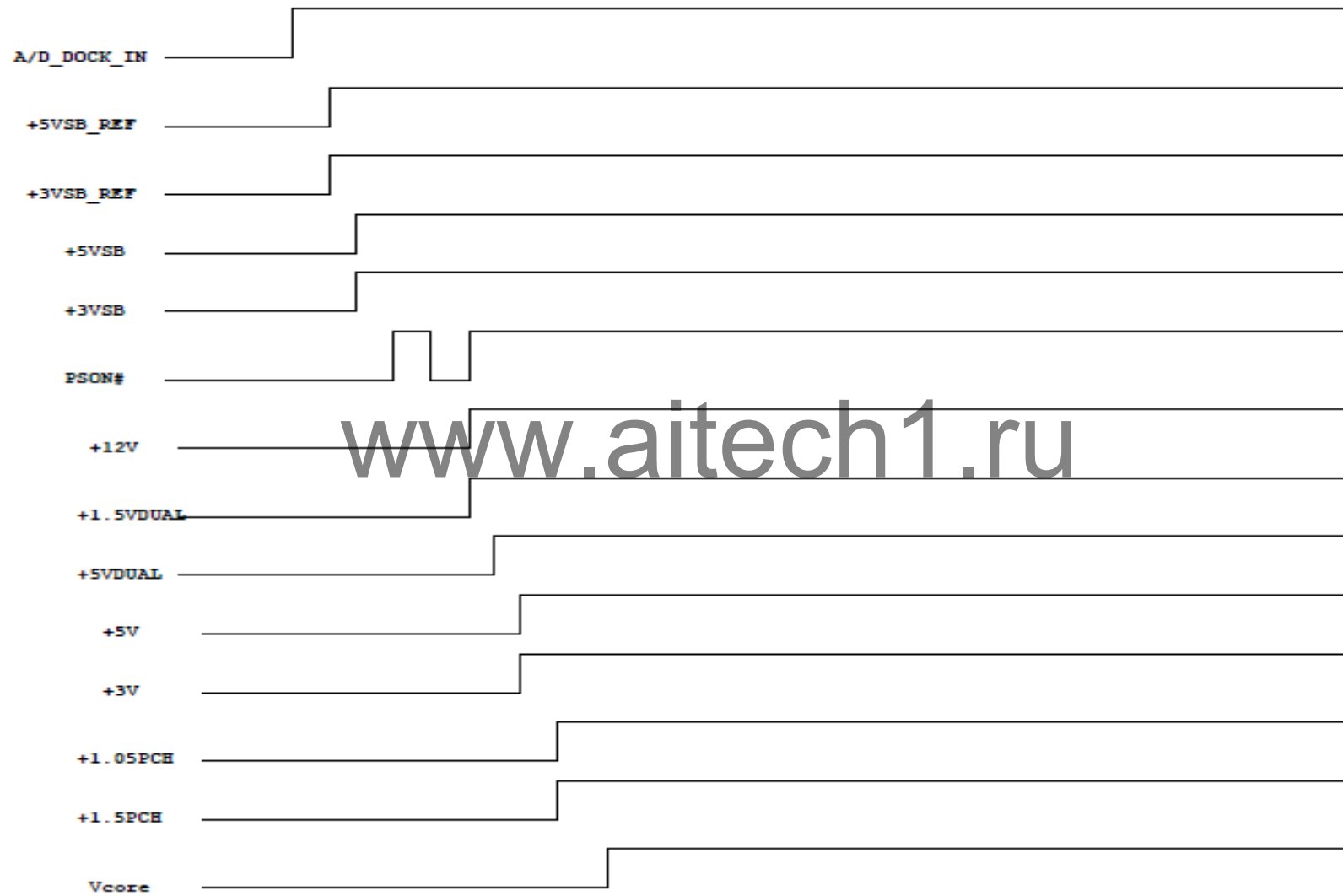
BLOCK DIAGRAM



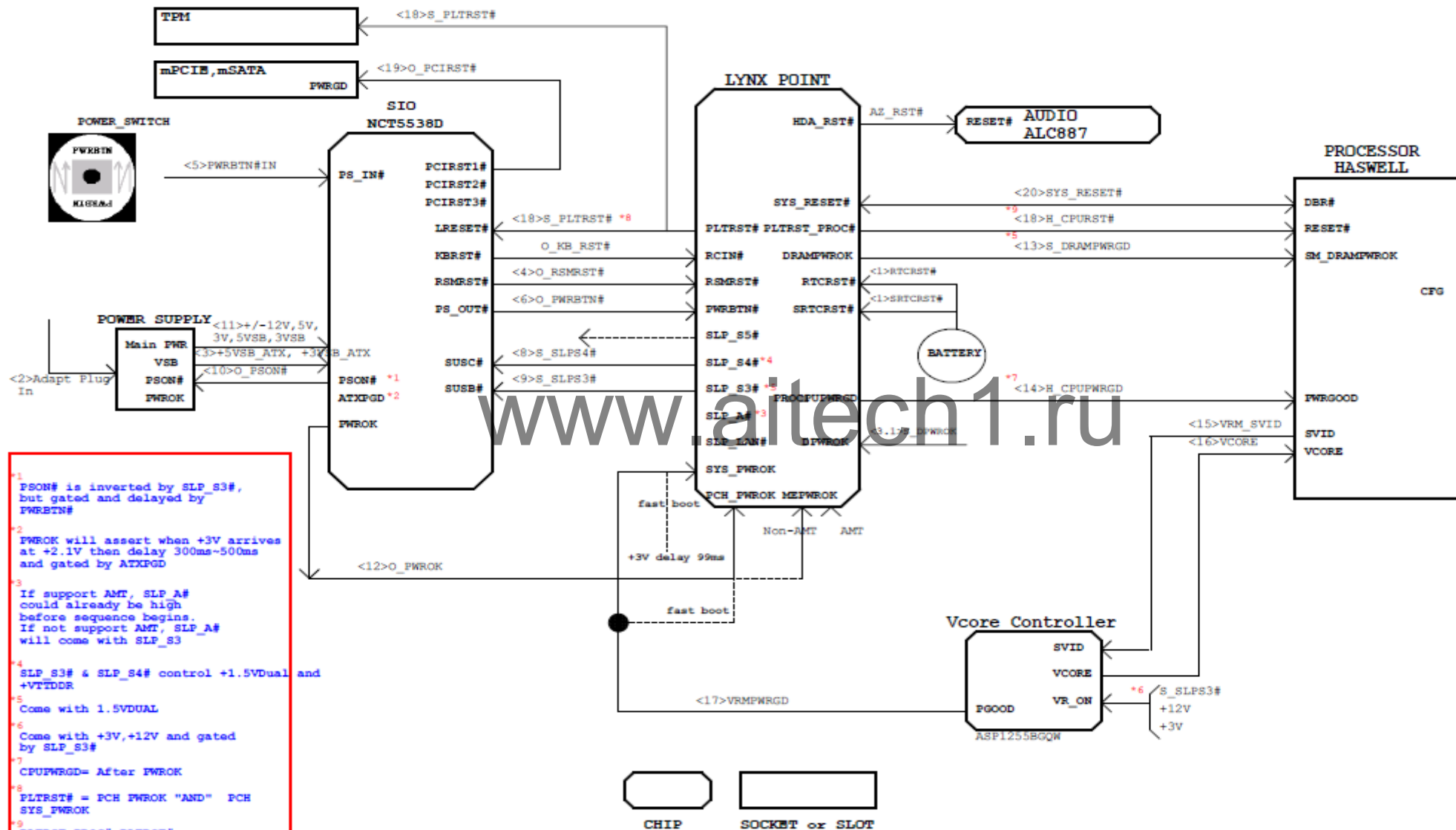
POWER FLOW



POWER FLOW

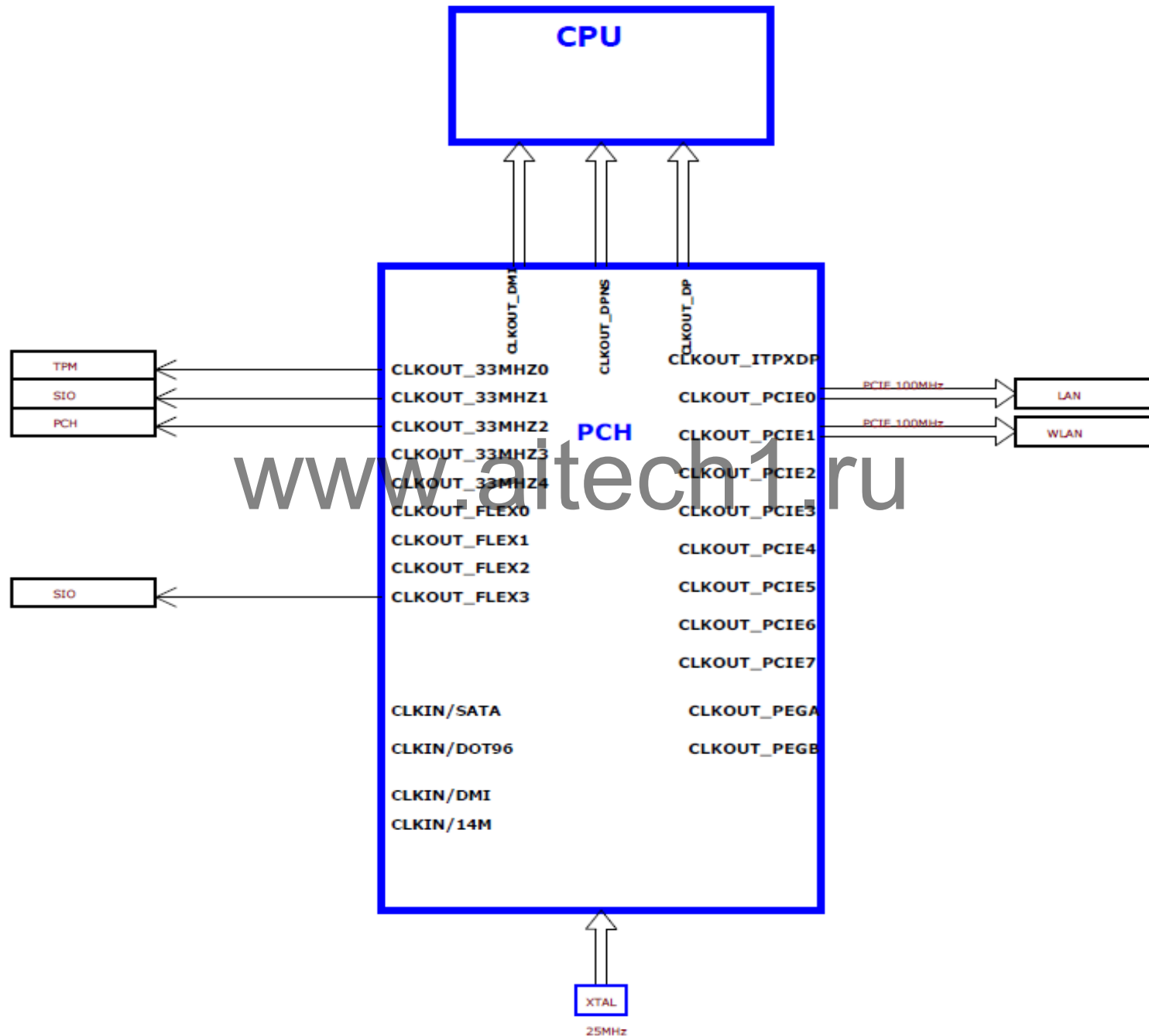


POWER ON SEQUENCE



- *1 PSON# is inverted by SLP_S3#, but gated and delayed by PWRBTN#
- *2 PWRON will assert when +3V arrives at +2.1V then delay 300ms-500ms and gated by ATXPGD
- *3 If support AMT, SLP_A# could already be high before sequence begins. If not support AMT, SLP_A# will come with SLP_S3
- *4 SLP_S3# & SLP_S4# control +1.5VDual and +VTTDDR
- *5 Come with 1.5VDUAL
- *6 Come with +3V, +12V and gated by SLP_S3#
- *7 CPUPWRGD= After PWRON
- *8 PLTRST# = PCH PWRON "AND" PCH SYS_PWRON
- *9 PLTRST_PROC# = PLTRST#, voltage=1V, directly connect to CPU

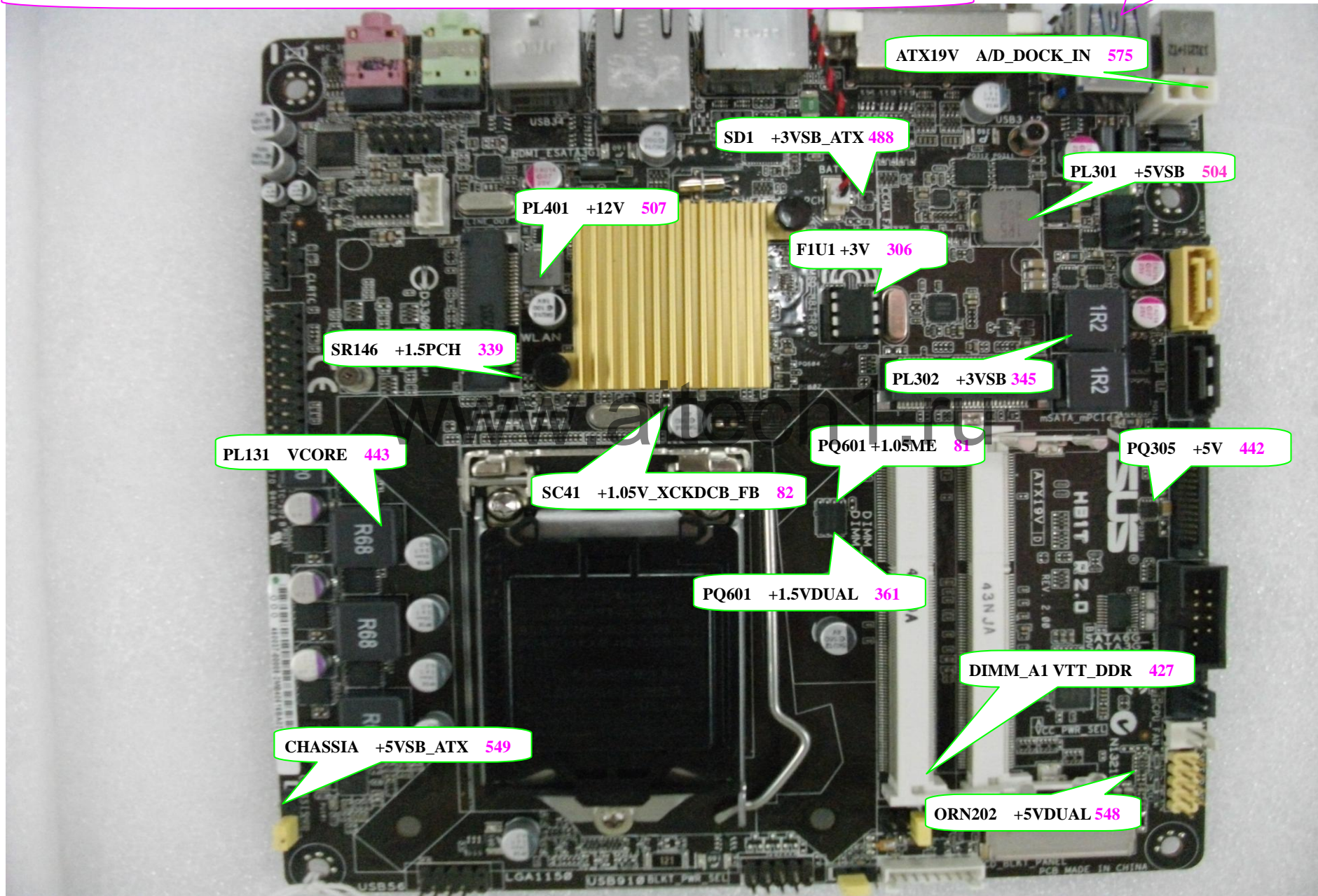
Frequency Flow



Voltage Measure Point

multi meter “VΩ mA” port touch GND

Pink number is Diode resistance to GND(without any part on MB)multimeter type DH-1240



Signal Measure Point

